AMENDED CLAIMS

1-54. (Canceled)

55. (Currently amended) A method of fabricating an interband tunnel diode, the method comprising the steps of:

layering a bottom injector;

layering a bottom spacer;

layering a top spacer;

layering a top injector adjacent to the bottom injector, the bottom injector and top injector forming a p-i-n junction; and

layering a material between the bottom injector and top ~~spacers~~ spacer which serves as a tunnel barrier, wherein the bottom injector layer, the top injector layer, and said material form a p-i-n junction, where i represents at least one material provided between the bottom injector and the top injector.

56-57. (Canceled)

58. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, wherein the layers in the interband tunnel diode are grown epitaxially.

59. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are a semiconductor or insulator.

60. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of a group IV alloy.

61. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, wherein the layers in the interband tunnel diode are grown epitaxially, wherein the epitaxial layers in the interband tunnel diode are comprised of, but not limited to, Si, Ge, C, Sn, $Si_{1-x}Ge_x$, $Si_{1-x}C_x$, $Si_{1-x}Sn_x$, $Si_{1-x-y}Ge_xC_y$, $Si_{1-x-y-z}Ge_xC_ySn_z$, $Si_{1-x}O_x$, $Si_{1-x}N_x$, $Al_{1-x}O_x$, or combinations thereof.

62. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, wherein the layers in the interband tunnel diode are grown in a molecular beam epitaxial (MBE) growth system.

63. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, wherein the layers in the interband tunnel diode are grown in a chemical vapor deposition (CVD) growth system.

64. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode.

65. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an inert or reducing atmospheres, or moreover a reduction in ambient gas pressure at a temperature in the range of 300 to 1000°C.

66. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 55, further comprising the step of heat treating the interband tunnel diode, during or after growth of the layers in the interband tunnel diode, using an inert or reducing atmosphere, or moreover a reduction in ambient gas pressure at a temperature in the range of 450 to 900°C.

67. (Withdrawn) The method of fabricating an interband tunnel diode as recited in claim 55, further comprising the step of heat treating the interband tunnel diode, during or after growth of ~~the~~ a bottom quantum well layer in the interband tunnel diode.

68. (Withdrawn) The method of fabricating an interband tunnel diode as recited in claim 55, further comprising the step of heat treating the interband tunnel diode, during or after growth of ~~the~~ top and bottom quantum well layers, the top and bottom spacer layers, or the tunnel barrier in the interband tunnel diode.

69. (Original) The method of fabricating an interband tunnel diode as recited in claim 58, wherein the epitaxial growth system occurs over a substrate temperature range between 50°C and 900°C during growth of the layers in the interband tunnel diode.

70. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of lowering a substrate temperature before or during growth of the bottom injector layer in the interband tunnel diode.

71. (Canceled)

72. (Previously presented) The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating a substrate temperature during or after growth of the bottom injector layer in the interband tunnel diode.

73. (Withdrawn) The method of fabricating an interband tunnel diode as recited in claim 58 further comprising the step of elevating a substrate temperature during or after growth of ~~the~~ a bottom quantum well in the interband tunnel diode.

74-88. (Canceled)

89. (Currently amended) The method ~~A method~~ of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 6 hours.

90. (Currently amended) The method ~~A method~~ of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 1 hour.

91. (Currently amended) The method ~~A method~~ of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 10 minutes.

92. (Currently amended) The method ~~A method~~ of fabricating an interband tunnel diode as recited in claim 64 by heat treating the diode for up to 2 minutes.